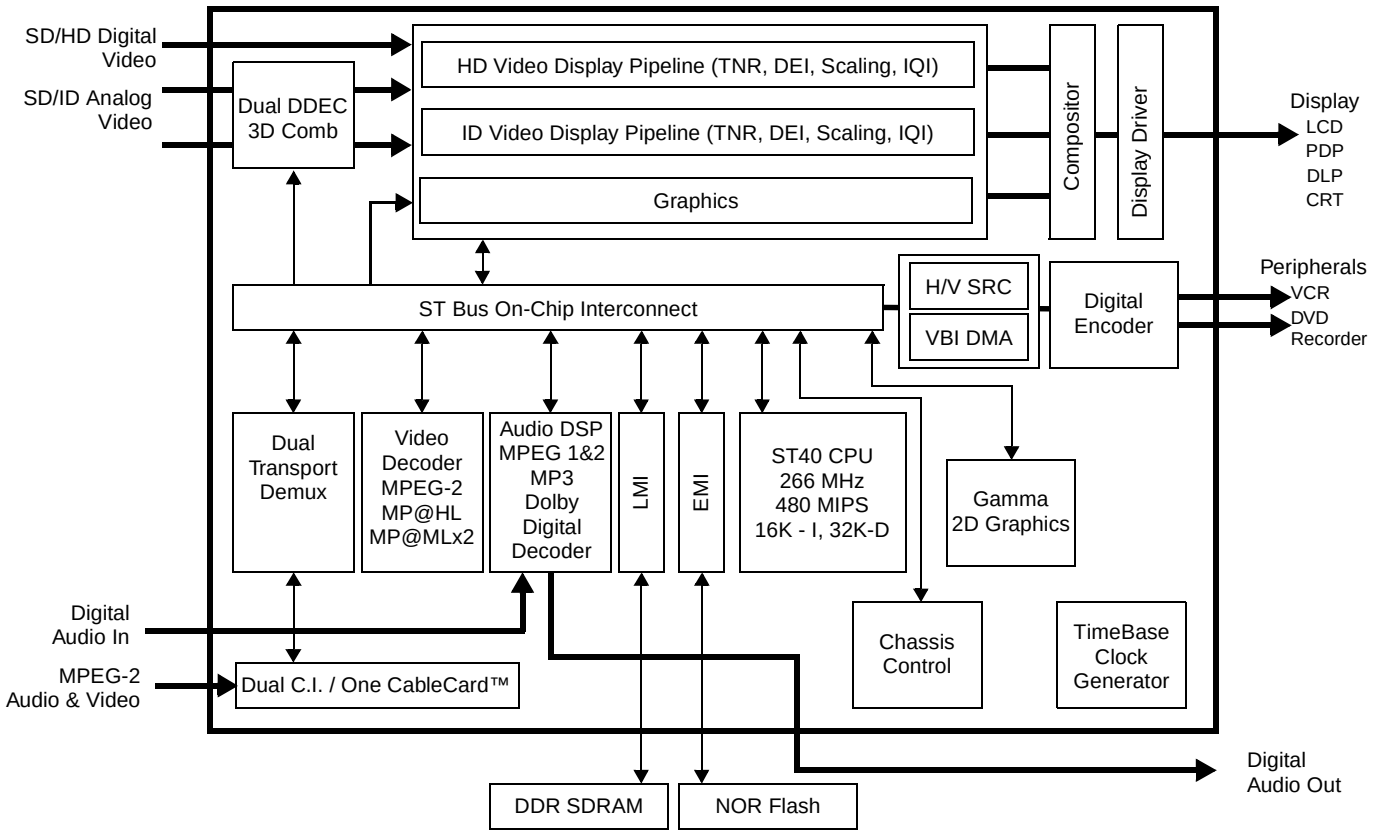
STD2000

Single-Chip Worldwide iDTV Processor

DATABRIEF



- **Dual-Channel High Definition Video Processor**
  - Up to 12-bit Video Processing
  - 3D Digital Luma/Chroma Noise Reduction
  - 3D Motion Adaptive Pixel-based Advanced Deinterlacing with Diagonal Compensation Contour Sensitive De-interlacing CSDi™
  - Flexible H/V Scaling Engine with Multi Window management capabilities
  - Image Quality Improvement Engine for crystal clear and crisp pictures
- **Dual Digital Chroma Decoder (PAL/SECAM/NTSC) with 3D/2D Comb Filter and Dual VBI Data Slicer**
- **Powerful 32-bit RISC ST40 CPU (266 MHz, 480 MIPS)**
- **Dual Transport Stream Demux with DES, DVB and Multi2 Descrambler**
- **Dual DVB-CI/one CableCARD™ interface**
- **MP@ML Dual Channel or MP@HL Single Channel MPEG-2 Video decoder**
- **24-bit audio DSP Core, MPEG-1 (Layers 1, 2 & 3), MPEG2, Dolby® Digital Decoder**
- **Gamma 2D Graphics Engine for Middleware graphics and On-Screen Display**
- **Auxiliary Video/Graphics Sub-System for Monitor output**
- **Exhaustive set of peripherals for DTV Chassis Control**
- **DDR333 Unified Memory Interface (LMI)**
- **Programmable External Memory Interface (EMI)**
- **CRT and Flat Panel Display Video Outputs**
- **27 MHz Crystal Oscillator**

Dual Channel Video Input Processor

■ **Analog Video Inputs**

- CVBS, Y/C, 1H/2H/2.14H YPrPb, 1H/2H RGB analog inputs

■ **Digital Video Inputs**

- D1/HD Digital video input (CCIR 601-656 / SMPTE 274M, SMPTE 296M, SMPTE 260M)
- YCL Digital video input (proprietary port; YCrCb-4:2:2, 2H for off-chip Motion-compensated Video Processing)
- RGB to YCrCb 4:2:2 conversion

■ **Analog Video Pre-Processing**

- Dual Digital Chroma Decoder (PAL/NTSC/SECAM)
- 3D Comb Filter support on one channel, adaptative 4H/2D comb filter on second channel
- Dual VBI data slicer for Teletext, CC, WSS and other systems
- 3:2/2:2 Pulldown, Video/Movie and Scene Change Detection
- 3D Digital Luma and Chroma Motion Adaptive Noise Reduction
- Automatic Letterbox Detection

Dual Channel High Definition Video Processor

■ **Image Processing**

- 24, 25, 30, 50, 60 to 50, 60, 75, 100, 120 Hz Field up-rate conversion
- 3D Motion-adaptive pixel-based advanced deinterlacing with diagonal compensation (CSDi™: Contour Sensitive Desinterlacer)

■ **Image Quality Improvements**

- LTI and CTI
- Contrast Enhancer: Black-White Stretch
- Blue Stretch
- Green Boost, Auto-Flesh and Tint Control
- Peaking: Adaptive Peaking and Coring

■ **Video Scaling & Composition**

- Horizontal/Vertical Format Conversion
- Support of 4:3 and 16:9 display aspect ratios
- Zoom In or Zoom out (X and Y independent linear factors from x0.25 to x4)
- Panoramic mode
- H or V crop and independent rescaling
- Compositor supporting Monochrome and Graphics planes
- Video two-channel HD processing for: PIP/POP, Picture And Picture (Perfect PAP), Picture In Graphic (PIG)

■ **Video Output Control**

- Color Space Translator (conversion to YCrCb 4:4:4 or RGB coding)
- Gamma Correction with programmable any-curve correction
- Perfect Color Engine (spatio-temporal dithering down to 4-to-8 bits)
- RGB 3x10-bit Digital output to flat panel or DMD
- RGB or YUV analog outputs
- Color warping for color gammut correction

CPU Sub-System

- 32-bit RISC ST40 CPU (266 MHz, 480MIPs)
- 16 Kbytes I-Cache and 32 Kbytes D-Cache RAM
- Floating Point Unit (FPU)
- Memory Management Unit (MMU)

■ **On-Chip Memory** (64 Kbytes SRAM)

■ **Services**

- Test Access Port and its link (JTAG based)
- Diagnostic Controller Unit (for low intrusion, real-time debugging)
- Advanced User Debug support
- System Bus Analyzer (SBAG)

Dual Transport Stream Processor

- Dual Transport Stream Demux
- DES, DVB and Multi2 descramblers
- Dual Transport processing: DVB or ATSC (ISO/IEC 13818-x and A53)
- DVB-CI interface (Dual Slot support)
- CableCARD™ interface (Single Slot support)

MPEG2 Digital Video Decoder

- MPEG2 Video (ISO/IEC 13818-2, ATSC-A54)
- MP@ML Dual-channel Decode or MP@HL Single-channel Decode
- Data Extraction (closed caption,...)

Digital Audio Decoder

- 24-bit audio DSP Core (with embedded Software & Patch RAM)
- MPEG1 (layers 1, 2 & 3), MPEG2, Dolby® Digital / ATSC-A52
- Lt/Rt Downmix for standard Stereo digital outputs
- Triple I²S channel outputs
- One PCM/Stream or I²S Input (S/PDIF external receiver or HDMI)
- S/PDIF Digital Output (IEC60958 and IEC61937)

Gamma 2D Graphic Processor

- Full Screen or windowed Bitmap area
- ARGB-4444 Graphics plane in mixed mode
- 2D-Graphics hardware accelerator
- GFx/Video programmable alpha-blending
- Background Color Plane
- Horizontal and/or Vertical Scrolling, controlled by software

Auxiliary Video/Graphics Processor

- On-chip PAL/NTSC/SECAM Encoder for monitor output
- Encoding of Teletext, WSS, VPS or Closed Caption
- Graphics plane for optional Subtitle support
- Macrovision Copy Protection (Factory Disable option)

DTV Chassis Control

- Two UARTs
- One Smartcard interface
- Two I²C (2 channels each)
- Four-channel PWM with input capture and compare
- Real-time Clock and WatchDog timer
- Infrared Receiver/Transmitter
- 10-bit, 8-channel low-speed A/D Converter
- 8 external interrupt channels with Interrupt Level Controller
- More than 56 General Purpose IOs
- Low-power mode and wake-up controller

Interfaces

- **Local Memory Interface (LMI)**
  - 64-bit, dual-port DDR memory interface
  - 16- and 32-bit DDR-SDRAM device support
  - Up to 166 MHz support
  - Support devices of up to 512 Mbits
- **Programmable External Memory Interface (EMI)**
  - 16-bit/8-bit External Memory Interface for supporting Flash and optional peripherals
  - Support NOR Flash devices of up to 256 Mbits
  - 6 separately configurable banks
  - Support for external memory-mapped ICs or sub-systems
- **FDP and CRT Video Outputs**
  - RGB 3x10-bit digital output to flat panel or DMD
  - RGB or YUV analog outputs for CRT

1 General Information

1.1 Introduction

The STD2000 is a highly-integrated, high performance system-on-chip iDTV processor that combines Set-top Box decoding facility with a powerful TV processor.

A dual-channel PIP/PAP video processor supports High Definition formats. Its advanced integration drastically reduces integrated Digital TV BOM costs by removing redundancy between Analog and Digital source video processing.

Compliant with worldwide standards such as ATSC, DVB-T, ISDB-T and the Chinese Digital Terrestrial Standard, the STD2000 also includes a built-in CableCARD™ interface for US OpenCable™ specifications and a dual DVB-CI interface for European DVB-T specifications.

1.2 Typical Applications

Typical applications for the STD2000 system-on-chip are illustrated in the following diagrams:

Figure 1: US LCD Digital Cable Ready HDTV

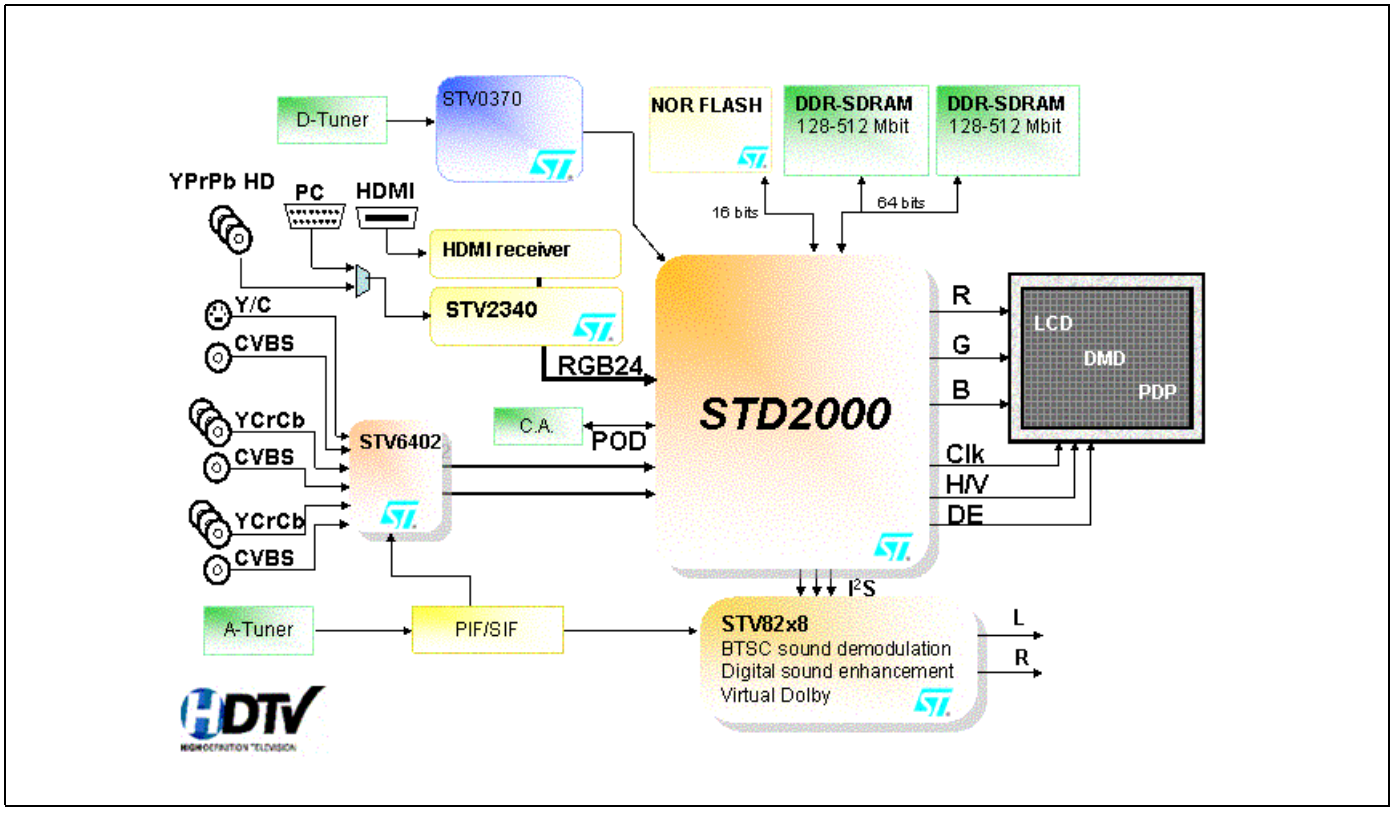


Figure 2: China CRT Digital Cable HDTV

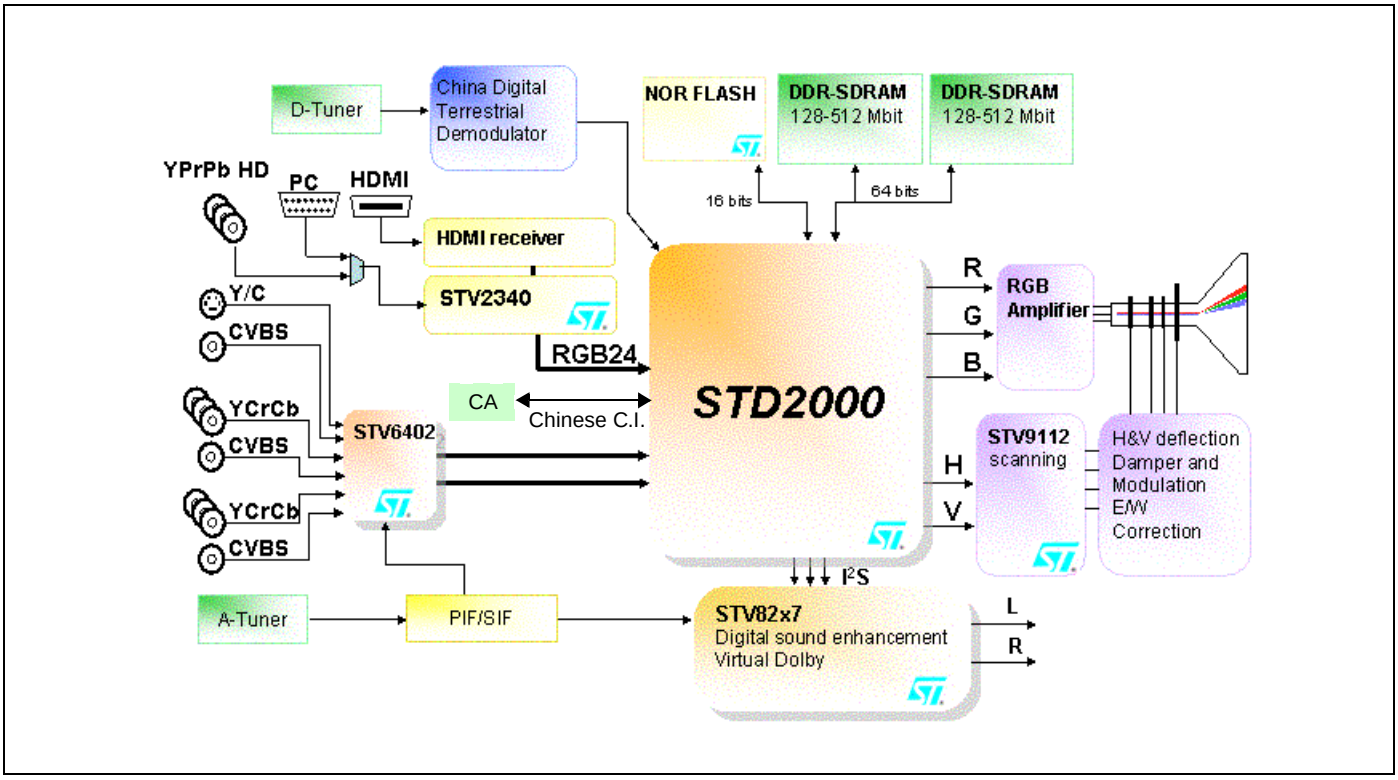
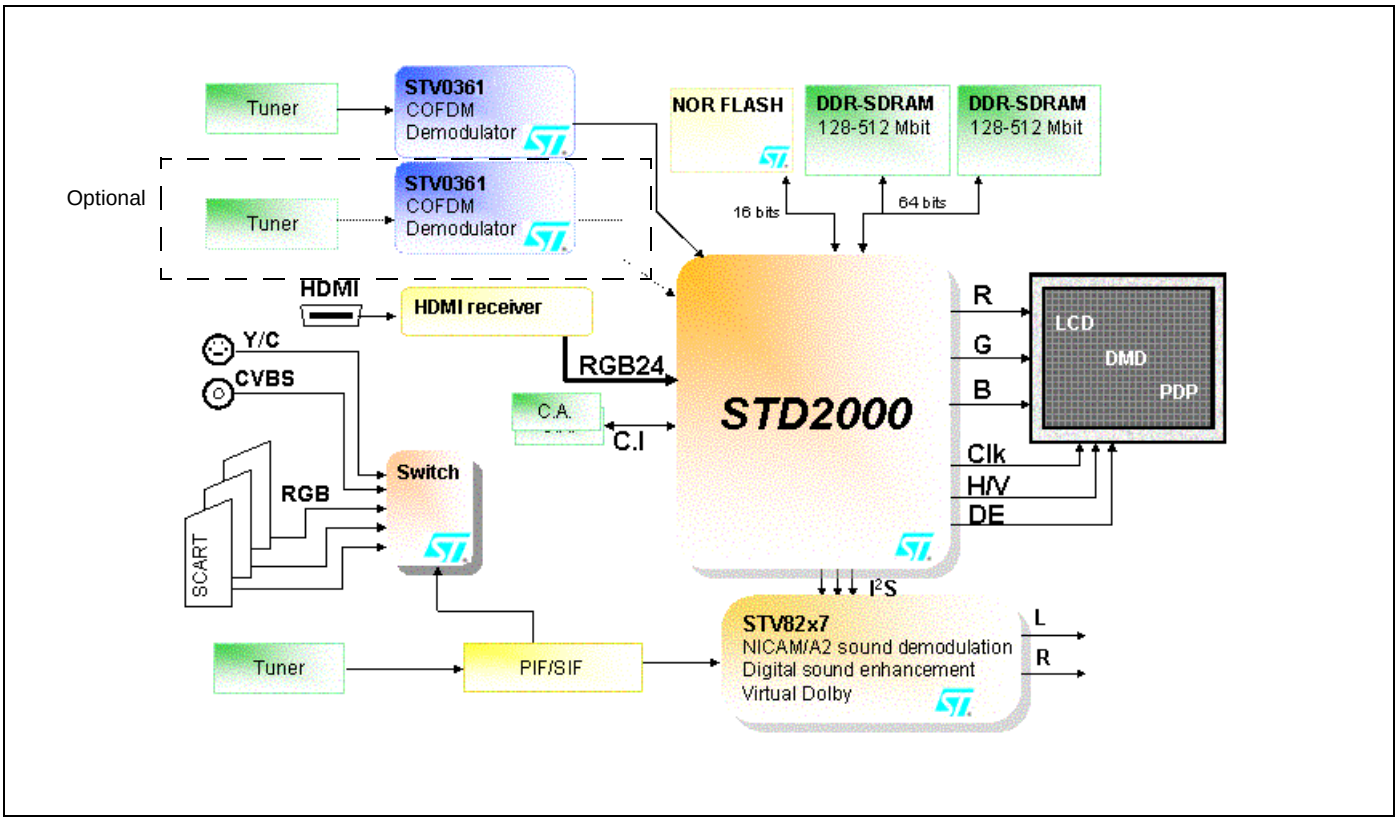


Figure 3: Europe LCD iDTV



2 STD2000 Pin List

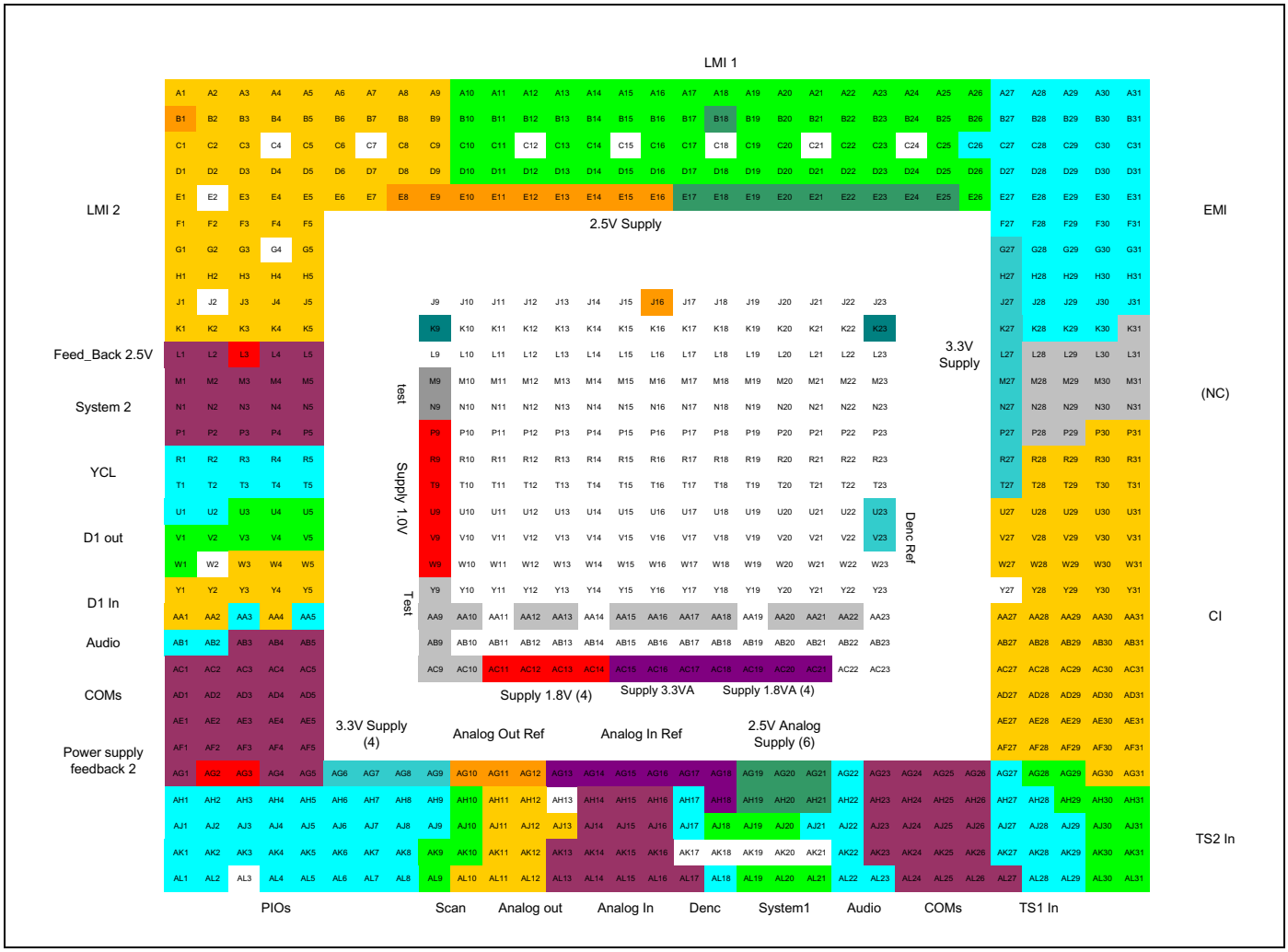
2.1 General Package Information

The STD2000 is delivered in a 745-ball BGA package.

Table 1: BGA Package Information

Package Type	MCM-BGA	
Body Size	40 x 40	mm
Ball Count	745	Balls
Ball Pitch	1.27	mm
Ball Matrix	31 x 31 (5-row perimeter)	Balls
Center Matrix	15 x 15	Balls

Figure 4: STD2000 Package Overview

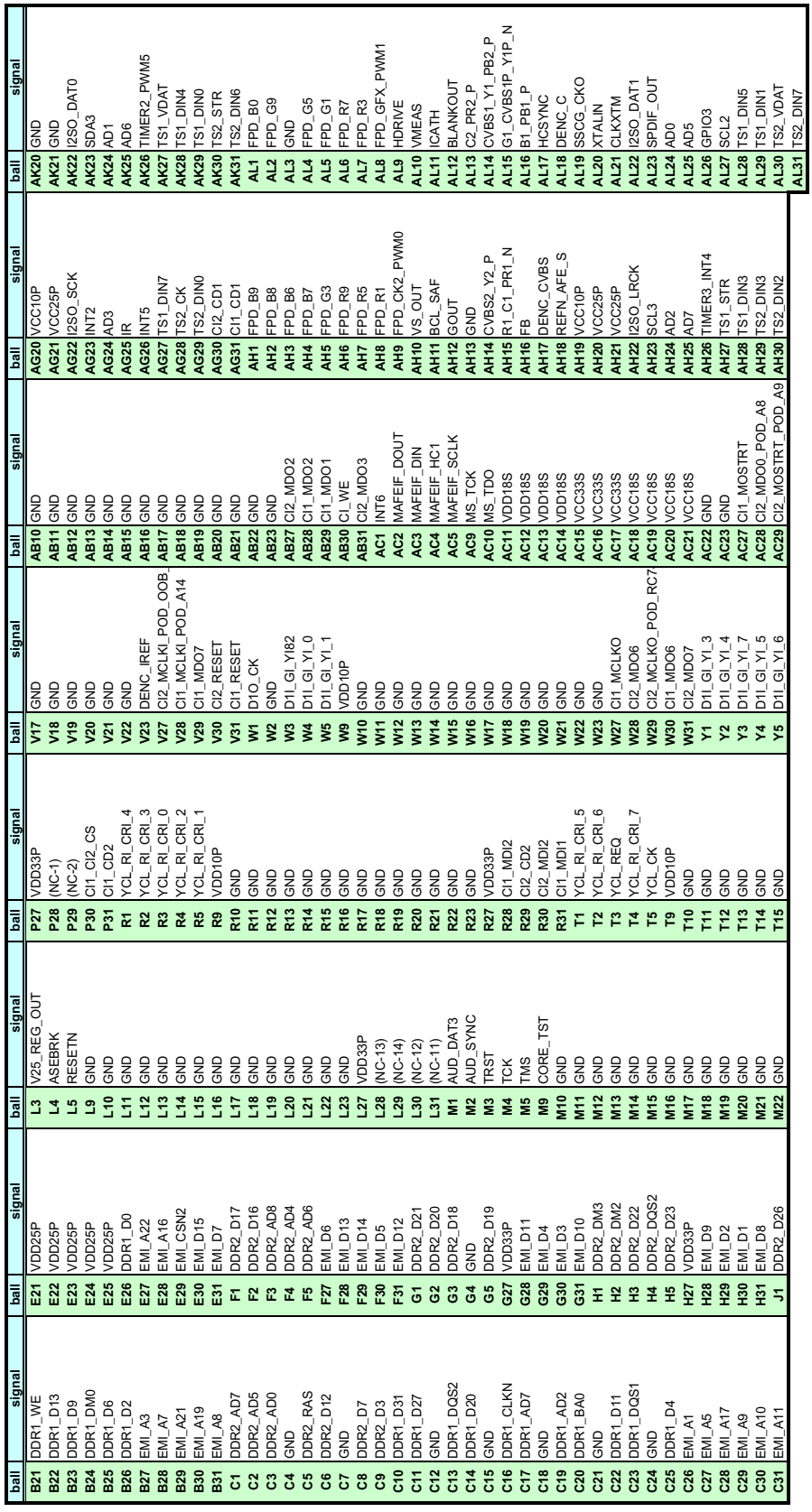


2.2 Ballout Description

Figure 5: Ballout Information (Part 1)

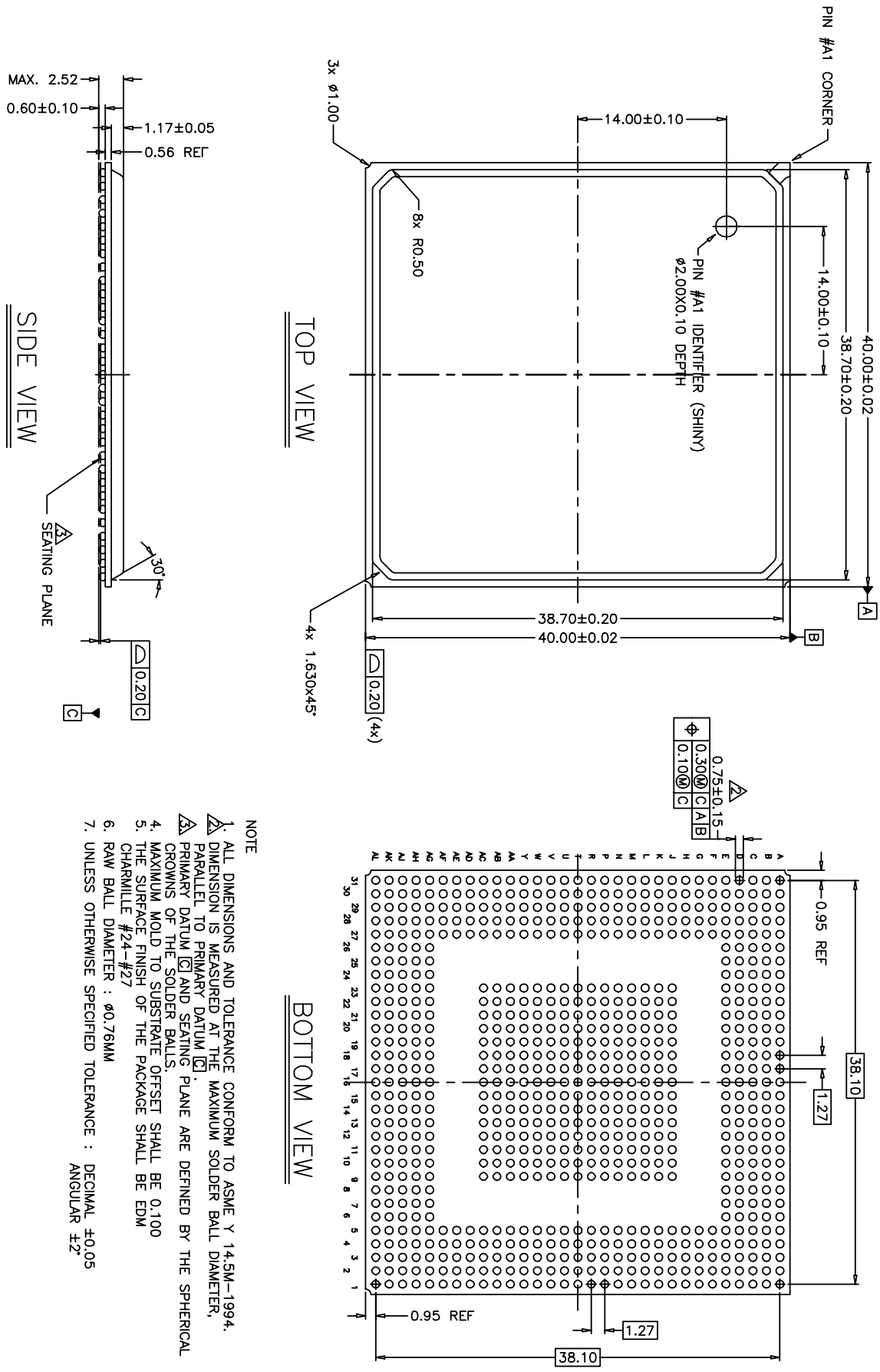
ball	signal	ball	signal	ball	signal	ball	signal	ball	signal	ball	signal	ball	signal
A1	DDR2_CAS	D1	DDR2_CLK	J2	GND	M23	GND	T16	GND	Y9	MS_TDI	AC30	CI1_MDO0	AH31	TS2_DIN1
A2	DDR2_BA1	D2	DDR2_AD12	J3	DDR2_DQS3	M27	VDD33P	T17	GND	Y10	GND	AC31	CI2_MDO1	AJ1	FPD_B5
A3	DDR2_AD3	D3	DDR2_AD9	J4	DDR2_D25	M28	(NC-9)	T18	GND	Y11	GND	AD1	MAFEIF_FSI	AJ2	FPD_B4
A4	DDR2_BA0	D4	DDR2_AD1	J5	DDR2_D24	M29	(NC-10)	T19	GND	Y12	GND	AD2	SC_CLK	AJ3	FPD_B3
A5	DDR2_D13	D5	DDR2_D15	J9	GND	M30	(NC-8)	T20	GND	Y13	GND	AD3	SC_DATA	AJ4	FPD_G7
A6	DDR2_D8	D6	DDR2_D10	J10	GND	M31	(NC-7)	T21	GND	Y14	GND	AD4	SC_RST	AJ5	FPD_G4
A7	DDR2_DQS0	D7	DDR2_DM1	J11	GND	N1	SBA_SYNC	T22	GND	Y15	GND	AD5	SC_CMD_VCC	AJ6	FPD_G0
A8	DDR2_D4	D8	DDR2_D6	J12	GND	N2	AUD_CK	T23	GND	Y16	GND	AD27	CI1_CE1_POD_CE2	AJ7	FPD_R6
A9	DDR2_D0	D9	DDR2_D2	J13	GND	N3	AUD_DAT2	T27	VDD33P	Y17	GND	AD28	CI_OE	AJ8	FPD_R2
A10	DDR1_D28	D10	DDR1_D30	J14	GND	N4	AUD_DAT0	T28	CI2_MDI0	Y18	GND	AD29	CI2_CE1_POD_CE1	AJ9	FPD_DE_PWM3
A11	DDR1_D24	D11	DDR1_D26	J15	GND	N5	AUD_DAT1	T29	CI1_MISTRT	Y19	GND	AD30	CI_IORD	AJ10	HOUTA_PWM2
A12	DDR1_DM2	D12	DDR1_DQS3	J16	DDR_REXT	N9	VPP	T30	CI1_MDI0	Y20	GND	AD31	CI_IOWR	AJ11	HCLKVBK
A13	DDR1_D21	D13	DDR1_D23	J17	GND	N10	GND	T31	CI2_MDI1	Y21	GND	AE1	SC_DETECT	AJ12	ROUT
A14	DDR1_D17	D14	DDR1_D19	J18	GND	N11	GND	U1	YCL_VAL	Y22	GND	AE2	CDA_REQ_RXD	AJ13	SVM
A15	DDR1_AD6	D15	DDR1_D16	J19	GND	N12	GND	U2	YCL_VSYNC	Y23	GND	AE3	CDA_DAT_CTS	AJ14	CVBS2_Y2_N
A16	DDR1_AD8	D16	DDR1_CKE	J20	GND	N13	GND	U3	D1O_BI_CBI_2	Y27	GND	AE4	CDA_CK_TXD	AJ15	R1_C1_PR1_P
A17	DDR1_CLK	D17	DDR1_AD9	J21	GND	N14	GND	U4	D1O_BI_CBI_0	Y28	CI1_MOVAL	AE5	CDA_DVAL_RTS	AJ16	VSYNC
A18	DDR1_AD5	D18	DDR1_CAS	J22	GND	N15	GND	U5	D1O_BI_CBI_1	Y29	CI2_MOVAL	AE27	CI2_MDI6	AJ17	DENC_Y
A19	DDR1_CS	D19	DDR1_AD0	J23	GND	N16	GND	U9	VDD10P	Y30	CI2_MDO5	AE28	CI1_MDI6	AJ18	SSCG_CKI
A20	DDR1_AD3	D20	DDR1_AD10	J27	VDD33P	N17	GND	U10	GND	Y31	CI1_MDO5	AE29	CI1_MDI5	AJ19	XTALOUT
A21	DDR1_RAS	D21	DDR1_D15	J28	EMI_OE	N18	GND	U11	GND	AA1	D1I_HD_CK	AE30	CI2_MDI7	AJ20	CLKXTP
A22	DDR1_D14	D22	DDR1_D12	J29	EMI_D0	N19	GND	U12	GND	AA2	D1I_HD_HSYNC	AE31	CI1_MDI7	AJ21	I2SO_DAT2
A23	DDR1_D10	D23	DDR1_D8	J30	EMI_FLA_CSN	N20	GND	U13	GND	AA3	I²SI_SCK	AF1	INT0	AJ22	I2SO_MCK
A24	DDR1_DM1	D24	DDR1_DQS0	J31	EMI_A0	N21	GND	U14	GND	AA4	D1I_HD_VSYNC	AF2	INT1	AJ23	INT3
A25	DDR1_D7	D25	DDR1_D5	K1	DDR2_D31	N22	GND	U15	GND	AA5	I²SI_LRCK	AF3	GPIO2	AJ24	AD4
A26	DDR1_D3	D26	DDR1_D1	K2	DDR2_D30	N23	GND	U16	GND	AA9	MS_TMS	AF4	GPIO0	AJ25	TIMER0_BLAST_OUT
A27	EMI_A2	D27	EMI_A4	K3	DDR2_D27	N27	VDD33P	U17	GND	AA10	MS_TSTRSTN	AF5	GPIO1	AJ26	SDA2
A28	EMI_A6	D28	EMI_A13	K4	DDR2_D29	N28	(NC-5)	U18	GND	AA11	GND	AF27	CI1_MDI3	AJ27	TS1_DIN6
A29	EMI_A18	D29	EMI_A12	K5	DDR2_D28	N29	(NC-6)	U19	GND	AA12	MS_SCANMODE	AF28	CI2_MDI4	AJ28	TS1_DIN2
A30	EMI_R/WN	D30	EMI_A14	K9		N30	(NC-4)	U20	GND	AA13	MS_TSTMODE	AF29	CI2_MDI3	AJ29	TS1_CK
A31	EMI_A20	D31	EMI_A15	K10	GND	N31	(NC-3)	U21	GND	AA14	GND	AF30	CI1_MDI4	AJ30	TS2_DIN5
B1	DDR2_VREF	E1	DDR2_AD11	K11	GND	P1	SBA_CK	U22	GND	AA15	TST_AFE0	AF31	CI2_MDI5	AJ31	TS2_DIN4
B2	DDR2_CS	E2	GND	K12	GND	P2	SBA_DAT0	U23	DENC_VREF	AA16	TST_AFE1	AG1	TIMER1_PWM4	AK1	FPD_B2
B3	DDR2_AD2	E3	DDR2_CLKN	K13	GND	P3	SBA_DAT3	U27	CI1_WAIT	AA17	TST_AFE2	AG2	V10_REG_OUT	AK2	FPD_B1
B4	DDR2_AD10	E4	DDR2_CKE	K14	GND	P4	SBA_DAT1	U28	CI2_MIVAL	AA18	TST_AFE3	AG3	V18_REG_OUT	AK3	FPD_G8
B5	DDR2_D14	E5	DDR2_WE	K15	GND	P5	SBA_DAT2	U29	CI2_WAIT	AA19	GND	AG4	SDA0	AK4	FPD_G6
B6	DDR2_D9	E6	DDR2_D11	K16	GND	P9	VDD10P	U30	CI1_MIVAL	AA20	MS_TSTCK27	AG5	SCL0	AK5	FPD_G2
B7	DDR2_DM0	E7	DDR2_DQS1	K17	GND	P10	GND	U31	CI2_MISTRT_POD_OOB	AA21	MS_TSTCK54	AG6	VDD33S	AK6	FPD_R8
B8	DDR2_D5	E8	VDD25P	K18	GND	P11	GND	V1	D1O_BI_CBI_3	AA22	MS_TSTCK81	AG7	VDD33S	AK7	FPD_R4
B9	DDR2_D1	E9	VDD25P	K19	GND	P12	GND	V2	D1O_BI_CBI_4	AA23	GND	AG8	VDD33S	AK8	FPD_R0
B10	DDR1_D29	E10	VDD25P	K20	GND	P13	GND	V3	D1O_BI_CBI_7	AA27	CI2_IREQ	AG9	VDD33S	AK9	FPD_CK1_VFLYBACK
B11	DDR1_D25	E11	VDD25P	K21	GND	P14	GND	V4	D1O_BI_CBI_5	AA28	CI1_IREQ	AG10	IREF_ABE	AK10	HS_OUT
B12	DDR1_DM3	E12	VDD25P	K22	GND	P15	GND	V5	D1O_BI_CBI_6	AA29	CI1_MDO3	AG11	GNDREF_ABE	AK11	DPC
B13	DDR1_D22	E13	VDD25P			P16	GND	V9	VDD10P	AA30	CI2_MDO4	AG12	VREF_ABE	AK12	BOUT
B14	DDR1_D18	E14	VDD25P	K27	VDD33P	P17	GND	V10	GND	AA31	CI1_MDO4	AG13	REFP_AFE_F	AK13	C2_PR2_N
B15	DDR1_AD4	E15	VDD25P	K28	EMI_CSN0	P18	GND	V11	GND	AB1	I²SI_MCK	AG14	REFN_AFE_F	AK14	CVBS1_Y1_PB2_N
B16	DDR1_AD11	E16	VDD25P	K29	EMI_CSN1	P19	GND	V12	GND	AB2	I²SI_DAT	AG15	RREF_AFE	AK15	G1_CVBS1P_Y1P_P
B17	DDR1_AD12	E17	VDD25P	K30	EMI_WAIT	P20	GND	V13	GND	AB3	INT7	AG16	RREF_GND_AFE	AK16	B1_PB1_N
B18	DDR1_VREF	E18	VDD25P	K31	(NC-15)	P21	GND	V14	GND	AB4	SDA1	AG17	VREF_AFE	AK17	GND
B19	DDR1_BA1	E19	VDD25P	L1	TDI	P22	GND	V15	GND	AB5	SCL1	AG18	REFP_AFE_S	AK18	GND
B20	DDR1_AD1	E20	VDD25P	L2	TDO	P23	GND	V16	GND	AB9	MS_TRST	AG19	VCC10P	AK19	GND

Figure 6: Ballout Information (Part 2)



ball	signal	ball	signal	ball	signal	ball	signal	ball	signal	ball	signal	ball	signal
B21	DDR1_WE	E21	VDD25P	L3	V25_REG_OUT	P27	VDD33P	V17	GND	AB10	GND	AG20	VCC10P	AK20	GND
B22	DDR1_D13	E22	VDD25P	L4	ASEBRK	P28	(NC-1)	V18	GND	AB11	GND	AG21	VCC25P	AK21	GND
B23	DDR1_D9	E23	VDD25P	L5	RESETN	P29	(NC-2)	V19	GND	AB12	GND	AG22	I2SO_SCK	AK22	I2SO_DAT0
B24	DDR1_DM0	E24	VDD25P	L9	GND	P30	CI1_CI2_CS	V20	GND	AB13	GND	AG23	INT2	AK23	SDA3
B25	DDR1_D6	E25	VDD25P	L10	GND	P31	CI1_CD2	V21	GND	AB14	GND	AG24	AD3	AK24	AD1
B26	DDR1_D2	E26	DDR1_D0	L11	GND	R1	YCL_RI_CRI_4	V22	GND	AB15	GND	AG25	IR	AK25	AD6
B27	EMI_A3	E27	EMI_A22	L12	GND	R2	YCL_RI_CRI_3	V23	DENC_IREF	AB16	GND	AG26	INT5	AK26	TIMER2_PWM5
B28	EMI_A7	E28	EMI_A16	L13	GND	R3	YCL_RI_CRI_0	V27	CI2_MCLKI_POD_OOB	AB17	GND	AG27	TS1_DIN7	AK27	TS1_VDAT
B29	EMI_A21	E29	EMI_CSN2	L14	GND	R4	YCL_RI_CRI_2	V28	CI1_MCLKI_POD_A14	AB18	GND	AG28	TS2_CK	AK28	TS1_DIN4
B30	EMI_A19	E30	EMI_D15	L15	GND	R5	YCL_RI_CRI_1	V29	CI1_MDO7	AB19	GND	AG29	TS2_DIN0	AK29	TS1_DIN0
B31	EMI_A8	E31	EMI_D7	L16	GND	R9	VDD10P	V30	CI2_RESET	AB20	GND	AG30	CI2_CD1	AK30	TS2_STR
C1	DDR2_AD7	F1	DDR2_D17	L17	GND	R10	GND	V31	CI1_RESET	AB21	GND	AG31	CI1_CD1	AK31	TS2_DIN6
C2	DDR2_AD5	F2	DDR2_D16	L18	GND	R11	GND	W1	D1O_CK	AB22	GND	AH1	FPD_B9	AL1	FPD_B0
C3	DDR2_AD0	F3	DDR2_AD8	L19	GND	R12	GND	W2	GND	AB23	GND	AH2	FPD_B8	AL2	FPD_G9
C4	GND	F4	DDR2_AD4	L20	GND	R13	GND	W3	D1I_GI_YI82	AB27	CI2_MDO2	AH3	FPD_B6	AL3	GND
C5	DDR2_RAS	F5	DDR2_AD6	L21	GND	R14	GND	W4	D1I_GI_YI_0	AB28	CI1_MDO2	AH4	FPD_B7	AL4	FPD_G5
C6	DDR2_D12	F27	EMI_D6	L22	GND	R15	GND	W5	D1I_GI_YI_1	AB29	CI1_MDO1	AH5	FPD_G3	AL5	FPD_G1
C7	GND	F28	EMI_D13	L23	GND	R16	GND	W9	VDD10P	AB30	CI_WE	AH6	FPD_R9	AL6	FPD_R7
C8	DDR2_D7	F29	EMI_D14	L27	VDD33P	R17	GND	W10	GND	AB31	CI2_MDO3	AH7	FPD_R5	AL7	FPD_R3
C9	DDR2_D3	F30	EMI_D5	L28	(NC-13)	R18	GND	W11	GND	AC1	INT6	AH8	FPD_R1	AL8	FPD_GFX_PWM1
C10	DDR1_D31	F31	EMI_D12	L29	(NC-14)	R19	GND	W12	GND	AC2	MAFEIF_DOUT	AH9	FPD_CK2_PWM0	AL9	HDRIVE
C11	DDR1_D27	G1	DDR2_D21	L30	(NC-12)	R20	GND	W13	GND	AC3	MAFEIF_DIN	AH10	VS_OUT	AL10	VMEAS
C12	GND	G2	DDR2_D20	L31	(NC-11)	R21	GND	W14	GND	AC4	MAFEIF_HC1	AH11	BCL_SAF	AL11	ICATH
C13	DDR1_DQS2	G3	DDR2_D18	M1	AUD_DAT3	R22	GND	W15	GND	AC5	MAFEIF_SCLK	AH12	GOUT	AL12	BLANKOUT
C14	DDR1_D20	G4	GND	M2	AUD_SYNC	R23	GND	W16	GND	AC9	MS_TCK	AH13	GND	AL13	C2_PR2_P
C15	GND	G5	DDR2_D19	M3	TRST	R27	VDD33P	W17	GND	AC10	MS_TDO	AH14	CVBS2_Y2_P	AL14	CVBS1_Y1_PB2_P
C16	DDR1_CLKN	G27	VDD33P	M4	TCK	R28	CI1_MDI2	W18	GND	AC11	VDD18S	AH15	R1_C1_PR1_N	AL15	G1_CVBS1P_Y1P_N
C17	DDR1_AD7	G28	EMI_D11	M5	TMS	R29	CI2_CD2	W19	GND	AC12	VDD18S	AH16	FB	AL16	B1_PB1_P
C18	GND	G29	EMI_D4	M9	CORE_TST	R30	CI2_MDI2	W20	GND	AC13	VDD18S	AH17	DENC_CVBS	AL17	HCSYNC
C19	DDR1_AD2	G30	EMI_D3	M10	GND	R31	CI1_MDI1	W21	GND	AC14	VDD18S	AH18	REFN_AFE_S	AL18	DENC_C
C20	DDR1_BA0	G31	EMI_D10	M11	GND	T1	YCL_RI_CRI_5	W22	GND	AC15	VCC33S	AH19	VCC10P	AL19	SSCG_CKO
C21	GND	H1	DDR2_DM3	M12	GND	T2	YCL_RI_CRI_6	W23	GND	AC16	VCC33S	AH20	VCC25P	AL20	XTALIN
C22	DDR1_D11	H2	DDR2_DM2	M13	GND	T3	YCL_REQ	W27	CI1_MCLKO	AC17	VCC33S	AH21	VCC25P	AL21	CLKXTM
C23	DDR1_DQS1	H3	DDR2_D22	M14	GND	T4	YCL_RI_CRI_7	W28	CI2_MDO6	AC18	VCC18S	AH22	I2SO_LRCK	AL22	I2SO_DAT1
C24	GND	H4	DDR2_DQS2	M15	GND	T5	YCL_CK	W29	CI2_MCLKO_POD_RC7	AC19	VCC18S	AH23	SCL3	AL23	SPDIF_OUT
C25	DDR1_D4	H5	DDR2_D23	M16	GND	T9	VDD10P	W30	CI1_MDO6	AC20	VCC18S	AH24	AD2	AL24	AD0
C26	EMI_A1	H27	VDD33P	M17	GND	T10	GND	W31	CI2_MDO7	AC21	VCC18S	AH25	AD7	AL25	AD5
C27	EMI_A5	H28	EMI_D9	M18	GND	T11	GND	Y1	D1I_GI_YI_3	AC22	GND	AH26	TIMER3_INT4	AL26	GPIO3
C28	EMI_A17	H29	EMI_D2	M19	GND	T12	GND	Y2	D1I_GI_YI_4	AC23	GND	AH27	TS1_STR	AL27	SCL2
C29	EMI_A9	H30	EMI_D1	M20	GND	T13	GND	Y3	D1I_GI_YI_7	AC27	CI1_MOSTRT	AH28	TS1_DIN3	AL28	TS1_DIN5
C30	EMI_A10	H31	EMI_D8	M21	GND	T14	GND	Y4	D1I_GI_YI_5	AC28	CI2_MDO0_POD_A8	AH29	TS2_DIN3	AL29	TS1_DIN1
C31	EMI_A11	J1	DDR2_D26	M22	GND	T15	GND	Y5	D1I_GI_YI_6	AC29	CI2_MOSTRT_POD_A9	AH30	TS2_DIN2	AL30	TS2_VDAT
														AL31	TS2_DIN7

3 Package Mechanical Data



NOTE

1. ALL DIMENSIONS AND TOLERANCE CONFORM TO ASME Y 14.5M–1994.
2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. MAXIMUM MOLD TO SUBSTRATE OFFSET SHALL BE 0.100
5. THE SURFACE FINISH OF THE PACKAGE SHALL BE EDM CHARMILLE #24–#27
6. RAW BALL DIAMETER : ø0.76MM
7. UNLESS OTHERWISE SPECIFIED TOLERANCE : DECIMAL ±0.05 ANGULAR ±2°

4 Revision History

Date	Revision	Changes
1-Mar-2005	1	Initial release
2-Jan 2006	2	Small changes applied to block diagram, features, figures 2 and 3.

NOTES: